II. REMARKS

Claims 1-23 are pending. The Applicants have amended claims 1-3, 5-8, 11, 13, 17-23. In light of the following, all of the claims as amended are now in condition for allowance.

Rejection of Claims 1-6 Under 35 U.S.C. § 102(b) in view of U.S. Patent 5,051,917 to Gould

Claim 1

Claim 1 as amended recites an integrated circuit having functional-circuit blocks, a region disposed between the functional-circuit blocks, and a transistor disposed in the region.

For example, referring, *e.g.*, to FIG. 1 of the patent application, an integrated circuit 10 includes functional circuit blocks 12, a region (the portion of the region 14 located outside of the blocks 12) disposed between the blocks, and an array 18 of one or more transistors disposed in the region.

Conversely, referring, *e.g.*, to Gould's FIG. 1 and column 4 lines 15-40, Gould does not disclose a transistor disposed in a region between functional-circuit blocks. Specifically, Gould discloses a standard cell chip 10 that includes blocks of inner cells 12 and blocks of outer cells 14, and a region (unlabeled) between these blocks. But Gould does not teach a transistor or any other circuit component disposed within this region.

Rejection of Claims 7-10 and 17-23 Under 35 U.S.C. § 103(a) in view of Gould

Claim 7

Gould neither teaches nor suggests a buffer disposed in a region between functional-circuit blocks. For example, referring, *e.g.*, to Gould's FIG. 1 and column 4 lines 15-40, Gould neither teaches nor suggests a buffer disposed in a region (unlabeled) between the blocks of inner cells 12 and the blocks of outer cells 14.

Claim 8

Gould neither teaches nor suggests a logic circuit disposed in a region between functional-circuit blocks. For example, referring, *e.g.*, to Gould's FIG. 1 and

column 4 lines 15-40, Gould neither teaches nor suggests a logic circuit disposed in a region (unlabeled) between the blocks of inner cells 12 and the blocks of outer cells 14.

Claim 17

Claim 17 is patentable for reasons similar to those discussed above in support of the patentability of claim 7.

Claim 20

Claim 20 is patentable for reasons similar to those discussed above in support of the patentability of claim 8.

Claim 21

Gould neither teaches nor suggests a transistor disposed in a region between functional-circuit blocks as discussed above in support of the patentability of claim 1.

Rejection of Claims 11-12 Under 35 U.S.C. § 103(a) in view of Gould and U.S. Patent 6,236,232 to Barnes

Claim 11

FIG. 1 of Barnes '232 is not a proper rejecting reference for claims 11-12. The present application is a CIP of Barnes '232, and the subject matter of claim 11 is fully supported by Barnes '232. Therefore, claim 11 is entitled to the same priority date as Barnes '232. Consequently, the effective date of Barnes '232 does not predate the priority date of claim 11.

Consequently, claim 11 is patentable over Gould for reasons similar to those discussed above in support of the patentability of claim 1.

And even if FIG. 1 of Barnes '232 is a proper rejecting reference, the combination of Gould and FIG. 1 of Barnes '232 does not obviate claim 11. Specifically, as discussed above in support of claim 1, Gould neither teaches nor suggests a transistor disposed in a region between functional-circuit blocks. Therefore, Gould would not have motivated one of skill in the art to locate a transistor (such as a transistor 102 or 104 of Barnes' FIG. 1) in a region between

functional-circuit blocks (such as in the unlabeled region between the blocks of inner cells 12 and the blocks of outer cells 14 in Gould's FIG. 1).

Rejection of Claims 13-16 Under 35 U.S.C. § 103(a) in view of Gould and U.S. Patent 6,414,518 to Patel

Claim 13

Claim 13 as amended recites an integrated circuit having a conductive path, functional-circuit blocks, one of which is coupled to the conductive path, a region located between the functional-circuit blocks, and a transistor disposed in the region and coupled to the conductive path.

For example, referring, *e.g.*, to FIGS. 1, 5A, and 5B of the patent application, an integrated circuit 10 includes functional circuit blocks 12, a region (the portion of the region 14 located outside of the blocks 12) disposed between the blocks, a conductive path 404 coupled to one of the blocks, and a transistor 402 disposed in the region 14 and coupled to the conductive path. For example, the transistor 402 may prevent a buildup of charge on the line 404 during processing of the circuit 10.

Conversely, referring, *e.g.*, to Gould's FIG. 1 and column 4 lines 15-40, and to Patel's FIG. 10C, the combination of Gould and Patel does not suggest a transistor disposed in a region between functional blocks and coupled to a conductive path. As discussed above in support of the patentability of claim 1, Gould does not teach a transistor disposed in a region between functional-circuit blocks. Specifically, Gould discloses a standard cell chip 10 that includes blocks of inner cells 12 and blocks of outer cells 14, and a region (unlabeled) between these blocks. But Gould does not teach a transistor or any other circuit component disposed in this region. And although Patel discloses a transistor 1062 having its terminals shorted together by a conductive path, Patel lacks the teaching missing from Gould, that is, disposing a transistor in a region between functional-circuit blocks. Consequently, Gould would not have motivated one of skill in the art to locate Patel's transistor 1062 in the region between Gould's blocks of cells 12 and 14.

Conclusion

In light of the foregoing, claims 1-23 as previously pending and claims 1-3, 5-8, 11, 13, 17-23 as amended are in condition for full allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 50-1078.

DATED this 18th day of March, 2003.

Respectfully Submitted,

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